amended Claim 9 to positively recite that conformal passivation layer 68 is positioned on the exposed sidewalls of emitter 66, patterned insulator layer 64 and a portion of SiGe base region 62; and that silicide regions 70 are located on exposed portions of SiGe layer 58, including SiGe base region 62, and emitter 66 not covered by conformal passivation layer 68. Support for the amendments made to Claim 9 is found in FIG 2 as well as at Page 5, line 1-Page 6, line 4 of the specification of the present application.

Since the above amendments to Claim 9 do not introduce new matter into the instant application, entry thereof is respectfully requested. Pursuant to 37 C.F.R. §1.121, applicants have attached a marked-up version of Claim 9 showing the changes made by the present amendment. The attachment is captioned as "**MARKED-UP VERSION SHOWING CHANGES MADE**".

In the present Office Action, Claims 1-17 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of applicants' admitted prior art, i.e., FIG 1, ("AAPA") in view of U.S. Patent No. 5,963,789 to Tsuchiaki ("Tsuchiaki").

The combination of AAPA and Tsuchiaki does not render applicants' claimed structure (or method) obvious since neither applied reference provides a structure (or method) wherein a conformal passivation layer is positioned (or formed) on exposed sidewalls of an emitter, a patterned insulator layer and a portion of a SiGe base region; and silicide regions which are located (or formed) on exposed portions of a SiGe layer, including portions of the SiGe base region, and the emitter not covered by the conformal passivation layer. Thus, in the claimed invention, the conformal passivation layer protects sidewalls of the emitter, patterned insulator and portions of the SiGe base region so that no silicide regions can be formed

thereon. The conformal passivation layer protects the structure in such a fashion that no shorts, i.e., silicide bridges, are formed in the structure.

The SiGe heterojunction bipolar transistor shown in FIG 1, i.e., the alleged AAPA, comprises semiconductor substrate 10 of a first conductivity type having sub-collector 14 and collector 16 formed therein. Isolation regions 12, which are also present in the substrate, define the outer boundaries of the bipolar transistor. The bipolar transistor of FIG 1 further includes SiGe layer 20 formed on a surface of substrate 10 as well as isolation regions 12. The SiGe layer includes polycrystalline Si regions 24 that are formed over the isolation regions and SiGe base region 22 that is formed over the collector and subcollector regions. The prior art bipolar transistor also includes patterned insulator layer 26 formed on the base region and emitter 28 formed on the patterned insulator layer as well as a surface of SiGe base region 22. Silicide regions 30 are also present in the structure shown in FIG 1. No conformal passivation layer is taught or suggest in AAPA, let alone the conformal passivation layer presently claimed which is located on exposed sidewalls of the emitter, the patterned insulator layer and a portion of the SiGe base region.

A major problem with the prior art SiGe heterojunction bipolar transistors of the type illustrated in FIG 1 is that the SiGe bipolar yield is significantly reduced because of the presence of shorts which are introduced into the structure during the silicide process. The shorts are caused by the presence of silicide bridges that exist in the structure. As such, a 20-30% yield loss is typically associated with prior art SiGe heterojunction bipolar transistors. The SiGe bipolar yield loss is more pronounced when cobalt disilicide regions are formed in the structure.

The above defects in AAPA are not alleviated by the disclosure of Tsuchiaki since the applied secondary reference also does not teach or suggest a structure (or method) including a conformal passivation layer positioned (or formed) on exposed sidewalls of an emitter, a patterned insulator layer and a portion of a SiGe base region; and silicide regions which are located on exposed portions of a SiGe layer, including portions of the SiGe base region, and the emitter not covered by the conformal passivation layer.

Tsuchiaki provides a method of manufacturing a semiconductor device having a thin foot region formed therein. The thin foot region (labeled as 206 in FIG 2C) is formed as follows: First, SiN film 201 is formed atop a surface of Si substrate 200, and thereafter patterned photoresist 200 is formed atop the SiN film. See FIG 2A. A reactive-ion etching step is then employed to provide the structure shown in FIG 2B. The structure shown includes an etched Si surface 205 as well as protective film 204 formed on the vertical sidewalls of Si substrate 200 which is protected by the patterned photoresist. Further etching is employed to provide the thin foot region in the structure.

As disclosed in Tsuchiaki, the passivation layer is formed *only* on vertical Si surfaces. There is no disclosure of forming the passivation layer on any other surface, let alone on exposed sidewalls of an emitter, a patterned insulator layer and a portion of a SiGe base region. Indeed, Tsuchiaki does not mention the presence of an emitter and a SiGe base region in the disclosed prior art structure. Applicants further submit that in Tsuchiaki, protective layer 204 is not taught or suggested as being formed on vertical sidewalls of SiN film 201. SiN is a well-known insulator material, thus the applied secondary reference teaches away from forming a passivation layer on sidewalls of an insulator.

Applicants also submit that in Tsuchiaki the protective film is removed after the thin foot region has been formed. In the claimed structure, the conformal passivation film remains on the structure and it is used to prevent the formation of silicide regions on regions that lay beneath the passivation film.

The §103 rejection also fails because there is no motivation in the applied references that suggests modifying the prior art structures or methods to include applicants' claimed passivation layer that is positioned on exposed sidewalls of an emitter, a patterned insulator layer as well as portions of a SiGe base region. The §103 rejection is thus improper since the prior art does not suggest this dramatic modification. The law requires that a prior art reference provide some teaching, suggestion or motivation to make the modification. In re Vaeck, 947 F.2d 488, 493, 20 USPQ 2d 1438, 1442 (Fed. Cir. 1991).

"The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. "In re Fritch, 972 F.2d 1260, 1266, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

There is no suggestion in the prior art of applicants' claimed method or structure recited in pending Claims 1-17. As such, the claims of the instant application are not obvious from any of the above-mentioned prior art references. Therefore, applicants respectfully submit that the rejection under 35 U.S.C. §103 has been obviated; and the withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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**ATTACHMENT: MARKED-UP VERSION SHOWING CHANGES MADE IN THE CLAIMS:**

Please amend Claim 9 to read as follows:

9. (Twice Amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region located therein, wherein said collector is located between isolation regions that are also present in the substrate;

a SiGe layer atop said substrate, said SiGe layer including polycrystalline Si regions positioned above said isolation regions and a SiGe base region located above said collector and subcollector regions;

a patterned insulator layer atop said SiGe base region, said patterned insulator having an opening therein;

an emitter located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a conformal passivation layer positioned on said exposed sidewalls of said emitter, said patterned insulator layer and a portion of said SiGe base region; and

silicide regions located on exposed portions of said SiGe layer, including portions of said SiGe base region, and said emitter not covered by said conformal passivation layer.